WHAT IS CLAIMED IS:

1. A clock regeneration circuit, comprising:

a PLL circuit which includes a voltage control oscillator, for synchronizing an oscillation frequency signal of the voltage control oscillator with a phase of a reception signal;

a clock extraction circuit which includes a band passing filter having a passing band width which concurrently extracts a basic waves component of the oscillation frequency signal of the voltage control oscillator and a harmonic component of a dividing signal of the oscillation frequency signal, for extracting a clock component of the reception signal;

a frequency detector for detecting a different in frequencies between an output of the clock extraction circuit and an oscillation frequency of the voltage control oscillator;

a filter for controlling the oscillation frequency of the voltage control oscillator of the PLL circuit at a detection output of the frequency detector;

a bit rate detection circuit for detecting a bit rate of the reception signal; and

a frequency selection circuit for outputting an oscillation frequency of the voltage control oscillator of the PLL circuit or a frequency signal obtained by dividing the oscillation frequency in response to the bit rate detected by the bit rate detection circuit, as a regeneration clock signal.

2. The clock regeneration circuit according to claim 1,

wherein

the clock extraction circuit further includes:

a delay circuit for delaying the reception signal by the half cycle; and

an EX-OR circuit for acquiring an exclusive OR operation of an output of the delay circuit and the reception signal, wherein

the output of the EX-OR circuit is led to the band passing filter in the configuration.

3. The clock regeneration circuit according to claim 1, wherein

the bit rate detection circuit includes:

a first AND gate for taking a conjunction of the reception signal and the oscillation frequency signal of the voltage control oscillator of the PLL circuit;

a delay circuit for delaying an output of the first AND gate by 1 cycle of the oscillation frequency signal of the voltage control oscillator;

a second AND gate for taking a conjunction of an output of the first AND gate and an output of the delay circuit; and

a circuit for acquiring an average value of the output of the AND gate.

4. The clock regeneration circuit according to claim 1, wherein

the bit rate detection circuit includes:

an AND gate for synthesizing the reception signal with a signal obtained by inverting the reception signal; and

a circuit for acquiring an average value of the output of the AND gate.

5. The clock regeneration circuit according to claim 1, wherein

the bit rate detection circuit includes:

an AND gate for synthesizing the reception signal with a signal obtained by inverting the reception signal; and

a circuit for counting a change point of the output of the AND gate.

6. An optical signal receiver, comprising:

a light receiving element for converting a received light signal into a reception electric signal;

a PLL circuit which includes a voltage control oscillator, for synchronizing an oscillation frequency signal of the voltage control oscillator with a phase of a reception electric signal;

a clock extraction circuit which includes a band passing filter having a passing band width which concurrently extracts a basic waves component of the oscillation frequency signal of the voltage control oscillator and a harmonic component of a dividing signal of the oscillation frequency signal, for extracting a clock component of the reception signal;

a frequency detector for detecting a difference in

frequencies between an output of the clock extraction circuit and an oscillation frequency of the voltage control oscillator;

a loop filter for controlling the oscillation frequency of the voltage control oscillator of the PLL circuit by a detection output of the frequency detector;

a discriminator for discriminating a level of the reception electric signal at a frequency timing of the output of the PLL circuit to output discrimination data;

a bit rate detection circuit for detecting a bit rate of the reception signal; and

a frequency selection circuit for outputting an oscillation frequency of the voltage control oscillator of the PLL circuit or a frequency signal obtained by dividing the oscillation frequency in response to the bit rate detected by the bit rate detection circuit, as a regeneration clock signal.

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